

184pin Unbuffered DDR DIMM Based on DDR400 32Mx8 SDRAM

Features

- 184-Pin Unbuffered Dual In-Line Memory Module
- 64Mx64 Unbuffered DDR DIMM based on 32Mx8 DDR SDRAM
- Performance:

	PC3200B	Unit
Speed Sort	-5T	
DIMM XAΣ Latency	3	
f CK Clock Frequency	200	MHz
t CK Clock Cycle	5	ns
f DQ DQ Burst Frequency	400	MHz

- Intended for 200 MHz applications
- Inputs and outputs are SSTL-2 compatible
- V_{DD} = 2.6Volt ± 0.1, V_{DDQ} = 2.6Volt ± 0.1
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges

- DRAM DLL aligns DQ and DQS transitions with clock transitions
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
 - DIMM XAΣ Latency: 2.5, 3
 - Burst Type: Sequential or Interleave
 - Burst Length: 2, 4, 8
 - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 13/10/2 Addressing (row/column/bank)
- 7.8 μs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 66-pin TSOP Type II Package

Description

M2U51264DS8HB3G-5T is an unbuffered 184-Pin Double Data Rate (DDR) Synchronous DRAM Dual In-Line Memory Module (DIMM), organized as a two-bank 64Mx64 high-speed memory array. The module uses sixteen 32Mx8 DDR SDRAMs in 400 mil TSOP II packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers.

The DIMM is intended for use in applications operating up to 200 MHz clock speeds and achieves high-speed data transfer rates of up to 400 MHz. Prior to any access operation, the device XAΣ latency and burst type/ length/operation type must be programmed into the DIMM by address inputs A0-A12 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed		Organization	Leads	Power
	200MHz (5ns @ CL = 3)	166MHz (6ns @ CL = 2.5)			
M2U51264DS8HB3G-5T	DDR400	PC3200	64Mx64	Gold	2.6V