512Mb DDR SDRAM

Features

CAS Latency and Frequency

CAS Latency	Maximum Operating Frequency (MHz)*	
	DDR400A (-5)*	DDR400B (-5T)
3	200	200
2.5	200	166

- Double data rate architecture: two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK and $\overline{CK}$)
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Burst lengths: 2, 4, or 8
- CAS Latency: 3, 2.5
- Auto Precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- 7.8µs Maximum Average Periodic Refresh Interval
- 2.5V (SSTL_2 compatible) I/O
- V_{DDQ} = 2.5V ± 0.2V
- V_{DD} = 2.5V ± 0.2V

Description

The 512Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The 512Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a *2n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR SDRAM effectively consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 512Mb DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going high and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4, or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving Power Down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Pin Configuration - 60 balls 0.8mmx1.0mm Pitch CSP Package

<Top View >

See the balls through the package.

128 X 4

1	2	3		7	8	9
VSSQ	NC	VSS	A	VDD	NC	VDDQ
NC	VDDQ	DQ3	B	DQ0	VSSQ	NC
NC	VSSQ	NC	C	NC	VDDQ	NC
NC	VDDQ	DQ2	D	DQ1	VSSQ	NC
NC	VSSQ	DQS	E	QFC	VDDQ	NC
VREF	VSS	DQM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

64 X 8

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VDD	DQ0	VDDQ
NC	VDDQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VDDQ	NC
NC	VDDQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	QFC	VDDQ	NC
VREF	VSS	DQM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

Pin Configuration - 60 balls 0.8mmx1.0mm Pitch CSP Package

<Top View >

See the balls through the package.

32 X 16

1	2	3		7	8	9
VSSQ	DQ15	VSS	A	VDD	DQ0	VDDQ
DQ14	VDDQ	DQ13	B	DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11	C	DQ4	VDDQ	DQ3
DQ10	VDDQ	DQ9	D	DQ6	VSSQ	DQ5
DQ8	VSSQ	DQS	E	LDQS	VDDQ	DQ7
VREF	VSS	DQM	F	LDW	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

Input/Output Functional Description

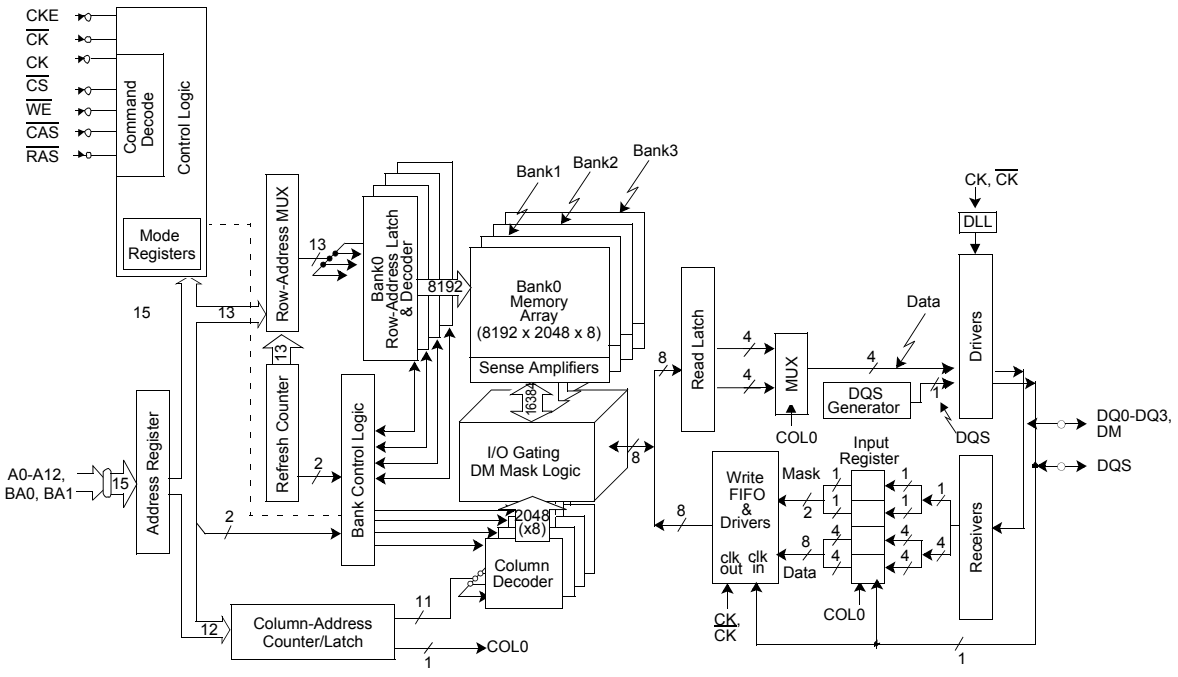
Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE, CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self Refresh operation (all banks idle), or Active Power Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during self refresh. The standard pinout includes one CKE pin. Optional pinouts might include CKE1 on a different pin, in addition to CKE0, to facilitate independent power down control of stacked devices.
$\overline{CS}$, $\overline{CS0}$, $\overline{CS1}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin. Optional pinouts might include $\overline{CS1}$ on a different pin, in addition to $\overline{CS0}$, to allow upper or lower deck selection on stacked devices.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. During a Read, DM can be driven high, low, or floated.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A12	Input	**Address Inputs:** Provide the row address for Active commands, and the column address and Auto Precharge bit for Read/Write commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 low) or all banks (A10 high). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a Mode Register Set command.
DQ	Input/Output	**Data Input/Output:** Data bus.
DQS, LDQS, UDQS	Input/Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15
NC		**No Connect:** No internal electrical connection is present.
NU		Electrical connection is present. Should not be connected at second level of assembly.
V_{DDQ}	Supply	**DQ Power Supply:** 2.5V ± 0.2V.
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.5V ± 0.2V.
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**SSTL_2 reference voltage:** (V_{DDQ} / 2) ± 1%.

Ordering Information

Org.	Part Number	Package	Speed				Comments
			Clock (MHz)	CL-t_{RCD}-t_{RP}	Clock (MHz)	CL-t_{RCD}-t_{RP}	
128M x 4	N2DS51240AF-5	60ball BGA 0.8mmx1.0mm Pitch	200	2.5-3-3	200	3-3-3	DDR400A
	N2DS51240AF-5T		200	3-3-3	166	2.5-3-3	DDR400B
64M x 8	N2DS51280AF-5	60ball BGA 0.8mmx1.0mm Pitch	200	2.5-3-3	200	3-3-3	DDR400A
	N2DS51280AF-5T		200	3-3-3	166	2.5-3-3	DDR400B
32M x 16	N2DS51216AF-5	60ball BGA 0.8mmx1.0mm Pitch	200	2.5-3-3	200	3-3-3	DDR400A
	N2DS51216AF-5T		200	3-3-3	166	2.5-3-3	DDR400B

Note:
1. At the present time, there are no plans to support DDR SDRAMs with the $\overline{QFC}$ function. All reference to $\overline{QFC}$ are for information only

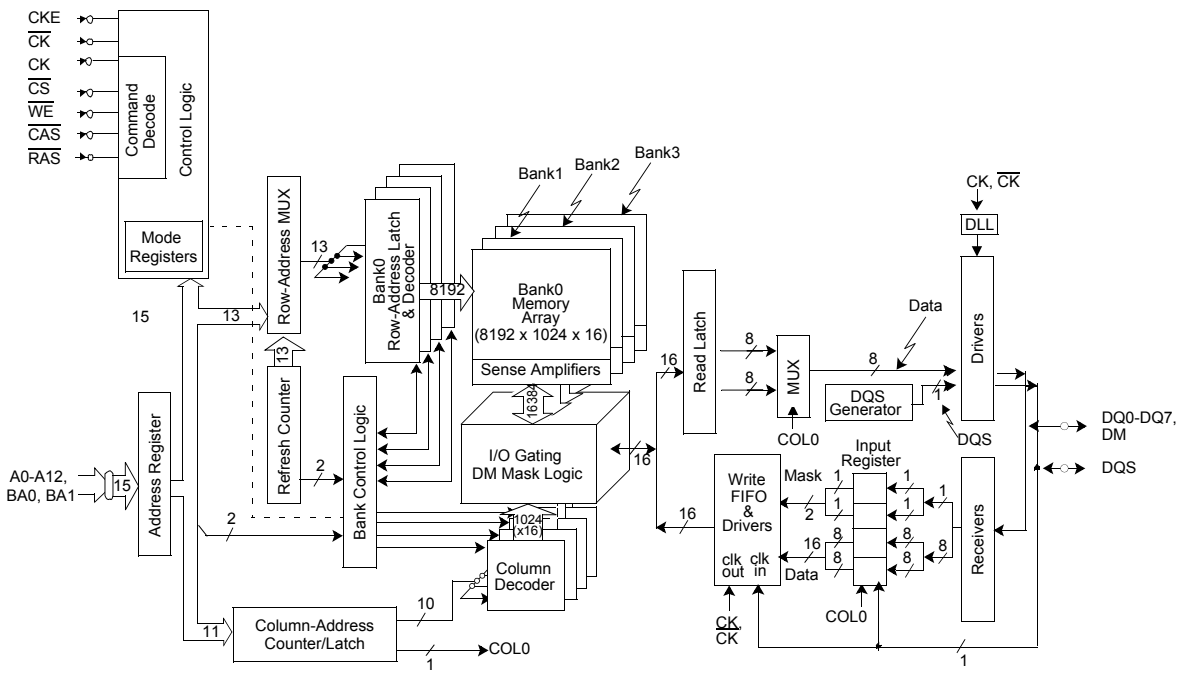
Block Diagram (128Mb x 4)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

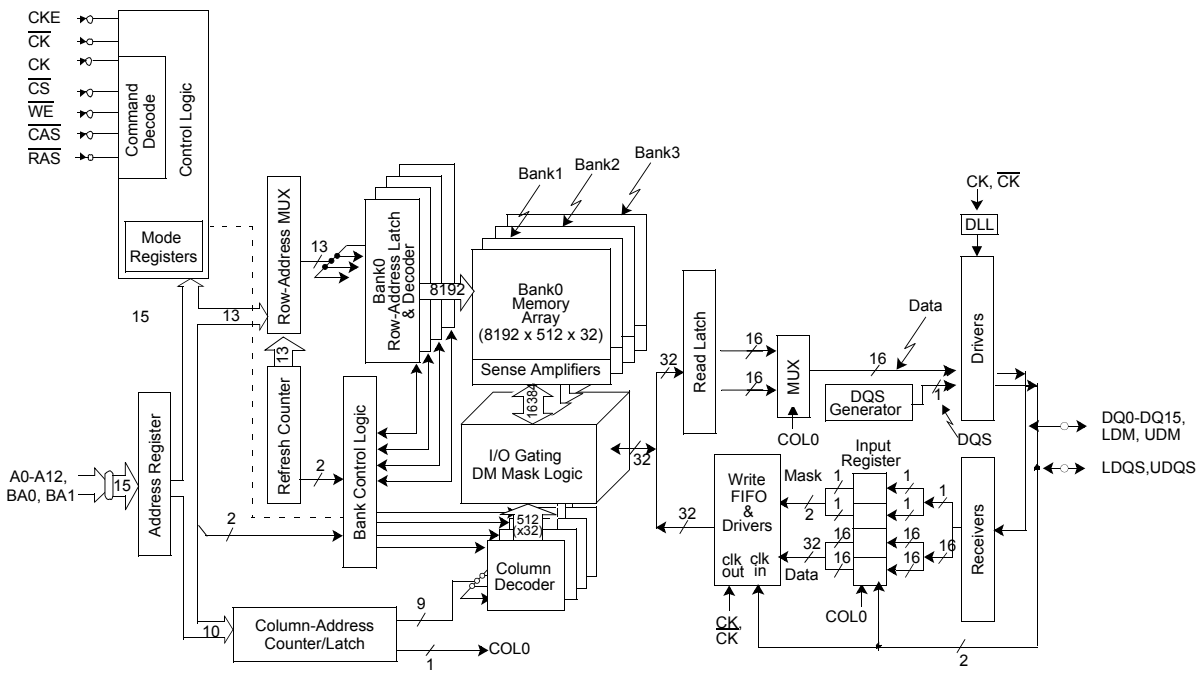
Block Diagram (64Mb x 8)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Block Diagram (32Mb x 16)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: UDM and LDM are unidirectional signals (input only), but is internally loaded to match the load of the bidirectional DQ, UDQS, and LDQS signals.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	−0.5 to V_{DDQ}+ 0.5	V
V_{IN}	Voltage on Inputs relative to V_{SS}	−0.5 to +3.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	−0.5 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	−0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	−55 to +150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DQS/DQ/DM Slew Rate

Parameter	Symbol	DDR400 (-5)		DDR400B (-5T)		Unit	Notes
		Min	Max	Min	Max		
DQS/DQ/DM input slew rate	DC_{SLEW}	TBD	TBD	TBD	TBD	V/ns	1, 2

1. Measured between V_{IH} (DC), V_{IL} (DC), and V_{IL} (DC), V_{IH} (DC).
2. DQS, DQ, and DM input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transition through the DC region must be monotonic.

Capacitance

Parameter	Symbol	Min.	Max.	Units	Notes
Input Capacitance: CK, $\overline{CK}$	CI_1	2.0	3.0	pF	1
Delta Input Capacitance: CK, $\overline{CK}$	delta CI_1		0.25	pF	1
Input Capacitance: All other input-only pins (except DM)	CI_2	2.0	3.0	pF	1
Delta Input Capacitance: All other input-only pins (except DM)	delta CI_2		0.5	pF	1
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	4.0	5.0	pF	1, 2
Delta Input/Output Capacitance: DQ, DQS, DM	delta C_{IO}		0.5	pF	1

1. $V_{DDQ} = V_{DD} = 2.5V \pm 0.2V$ (minimum range to maximum range), f = 100MHz, $T_A = 25^{\circ}C$, $VO_{DC} = V_{DDQ/2}$, $VO_{Peak\text{-}Peak} = 0.2V$.
2. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match input propagation times of DQ, DQS and DM in the system.

DC Electrical Characteristics and Operating Conditions

(0°C £ T_A £ 70×C; $V_{DDQ} = 2.5V \pm 0.2V$, V_{DD} = + 2.5V ± 0.2V, see AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage	2.3	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{TT}	I/O Termination Voltage (System)	V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
$V_{IH(DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
$V_{IL(DC)}$	Input Low (Logic0) Voltage	– 0.3	V_{REF} – 0.15	V	1
$V_{IN(DC)}$	Input Voltage Level, CK and $\overline{CK}$ Inputs	– 0.3	V_{DDQ} + 0.3	V	1
$V_{ID(DC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
$V_{IX(DC)}$	Input Crossing Point Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
VI_{Ratio}	V-I Matching Pullup Current to Pulldown Current Ratio	0.71	1.4		5
I_I	Input Leakage Current Any input $0V \le V_{IN} \le V_{DD}$; (All other pins not under test = 0V)	– 2	2	µA	1
I_{OZ}	Output Leakage Current (DQs are disabled; $0V \le V_{out} \le V_{DDQ}$	– 5	5	µA	1
I_{OH}	Output Current: Nominal Strength Driver High current (V_{OUT}= V_{DDQ} -0.373V, min V_{REF}, min V_{TT})	– 16.8		mA	1
I_{OL}	Low current (V_{OUT}= 0.373V, max V_{REF}, max V_{TT})	16.8			

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

DC Electrical Characteristics and Operating Conditions

(0°C £ T_A £ 70×C; V_{DDQ} = 2.5V ± 0.2V, V_{DD} = + 2.5V ± 0.2V, see AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
I_{OHW}	Output Current: Half- Strength Driver High current (V_{OUT}= V_{DDQ} -0.763V, min V_{REF}, min V_{TT})	– 9.0		mA	1
I_{OLW}	Low current (V_{OUT}= 0.763V, max V_{REF}, max V_{TT})	9.0			

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

Normal Strength Driver Pulldown and Pullup Currents

	Pulldown Current (mA)				Pullup Current (mA)			
Voltage (V)	Typical Low	Typical High	Min	Max	Typical Low	Typical High	Min	Max
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Normal Strength Driver Evaluation Conditions

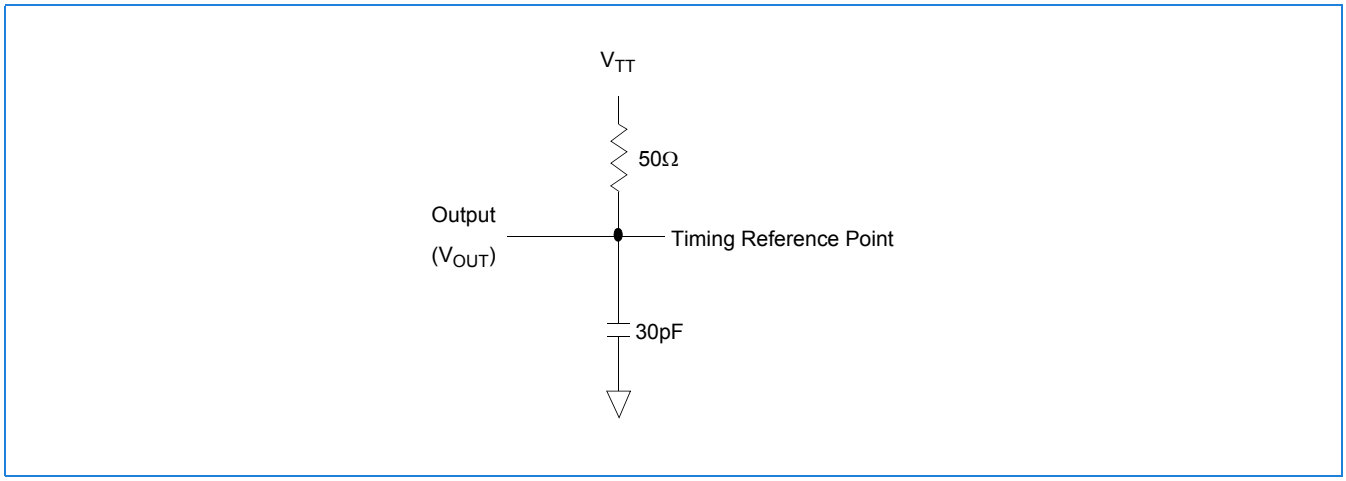
	Typical	Minimum	Maximum
Temperature ($T_{ambient}$)	25 °C	70 °C	0 °C
V_{DDQ}	2.5V	2.3V	2.7V
Process conditions	typical process	slow-slow process	fast-fast process

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input low (high) level.

AC Output Load Circuit Diagrams



AC Input Operating Conditions (0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH(AC)}$	Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	V_{REF} + 0.31		V	1, 2
$V_{IL(AC)}$	Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals		V_{REF} − 0.31	V	1, 2
$V_{ID(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.62	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX(AC)}$	Input Crossing Point Voltage, CK and $\overline{CK}$ Inputs	0.5*V_{DDQ} − 0.2	0.5*V_{DDQ} + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Electrical Characteristics & AC Timing - Absolute Specifications

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter		DDR400A (-5)		DDR400B (-5T)		Unit	Notes
			Min	Max	Min	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$		– 0.7	+ 0.7	– 0.75	+ 0.75	ns	1-4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		– 0.6	+ 0.6	– 0.75	+ 0.75	ns	1-4
t_{CH}	CK high-level width		0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CL}	CK low-level width		0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CK}	Clock cycle time	CL = 2.5	6	12	7.5	12	ns	1-4
		CL = 2.0	7.5	12	10	12		
t_{DH}	DQ and DM input hold time		0.45		0.5		ns	1-4, 15, 16
t_{DS}	DQ and DM input setup time		0.45		0.5		ns	1-4, 15, 16
t_{IPW}	Input pulse width		2.2		2.2		ns	2-4, 12
t_{DIPW}	DQ and DM input pulse width (each input)		1.75		1.75		ns	1-4
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$		– 0.7	+ 0.7	– 0.75	+ 0.75	ns	1-4, 5
t_{LZ}	Data-out low-impedance time from CK/$\overline{CK}$		– 0.7	+ 0.7	– 0.75	+ 0.75	ns	1-4, 5
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	TSOP Package		+ 0.45		+ 0.5	ns	1-4
		BGA Package		+ 0.4		+ 0.5	ns	1-4
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		t_{CK}	1-4
t_{QH}	Data output hold time from DQS		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{CK}	1-4
t_{QHS}	Data hold Skew Factor	TSOP Package		0.55		0.75	t_{CK}	1-4
		BGA Package		0.5		0.75	t_{CK}	1-4
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	t_{CK}	1-4
t_{DQSH}	DQS input high pulse width (write cycle)		0.35		0.35		t_{CK}	1-4
t_{DQSL}	DQS input low pulse width (write cycle)		0.35		0.35		t_{CK}	1-4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		t_{CK}	1-4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		t_{CK}	1-4
t_{MRD}	Mode register set command cycle time		2		2		t_{CK}	1-4
t_{WPRES}	Write preamble setup time		0		0		ns	1-4, 7
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	t_{CK}	1-4, 6
t_{WPRE}	Write preamble		0.25		0.25		t_{CK}	1-4
t_{IH}	Address and control input hold time (fast slew rate)		0.75		0.9		ns	2-4, 9, 11, 12
t_{IS}	Address and control input setup time (fast slew rate)		0.75		0.9		ns	2-4, 9, 11, 12
t_{IH}	Address and control input hold time (slow slew rate)		0.8		1.0		ns	2-4, 10, 11, 12, 14

Electrical Characteristics & AC Timing - Absolute Specifications

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	DDR400A (-5)		DDR400B (-5T)		Unit	Notes
		Min	Max	Min	Max		
t_{IS}	Address and control input setup time (slow slew rate)	0.8		1.0		ns	2-4, 10, 11, 12, 14
t_{RPRE}	Read preamble	0.9	1.1	0.9	1.1	t_{CK}	1-4
t_{RPST}	Read postamble	0.40	0.60	0.40	0.60	t_{CK}	1-4
t_{RAS}	Active to Precharge command	42	120,000	45	120,000	ns	1-4
t_{RC}	Active to Active/Auto-refresh command period	60		65		ns	1-4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period	72		75		ns	1-4
t_{RCD}	Active to Read or Write delay	18		20		ns	1-4
t_{RAP}	Active to Read Command with Autoprecharge	min (t_{RCD}, t_{RAS})		min (t_{RCD}, t_{RAS})		ns	1-4
t_{RP}	Precharge command period	18		20		ns	1-4
t_{RRD}	Active bank A to Active bank B command	12		15		ns	1-4
t_{WR}	Write recovery time	15		15		ns	1-4
t_{DAL}	Auto precharge write recovery + precharge time	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}	1-4, 13
t_{WTR}	Internal write to read command delay	1		1		t_{CK}	1-4
t_{PDEX}	Power down exit time	6		7.5		ns	1-4
t_{XSNR}	Exit self-refresh to non-read command	75		75		ns	1-4
t_{XSRD}	Exit self-refresh to read command	200		200		t_{CK}	1-4
t_{REFI}	Average Periodic Refresh Interval		7.8		7.8	µs	1-4, 8

Electrical Characteristics & AC Timing - Absolute Specifications Notes

1. Input slew rate = 1V/ns.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$ is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on t_{DQSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For command/address input slew rate $\geq$ 1.0V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
10. For command/address input slew rate $\geq$ 0.5V/ns and < 1.0V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
11. CK/$\overline{CK}$ slew rates are $\geq$ 1.0V/ns.
12. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
13. For each of the terms in parentheses, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time. For example, for DDR266B at CL = 2.5, t_{DAL} = (15ns/7.5ns) + (20ns/7.5ns) = 2 + 3 = 5.

14. An input setup and hold time derating table is used to increase t_{IS} and t_{IH} in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	delta (t_{IS})	delta (t_{IH})	Unit	Notes
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+50	0	ps	1,2
0.3 V/ns	+100	0	ps	1,2

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH\ (AC)}$ to $V_{IL\ (AC)}$ or $V_{IH\ (DC)}$ to $V_{IL\ (DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

15. An input setup and hold time derating table is used to increase t_{DS} and t_{DH} in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	delta (t_{DS})	delta (t_{DH})	Unit	Notes
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+75	+75	ps	1,2
0.3 V/ns	+150	+150	ps	1,2

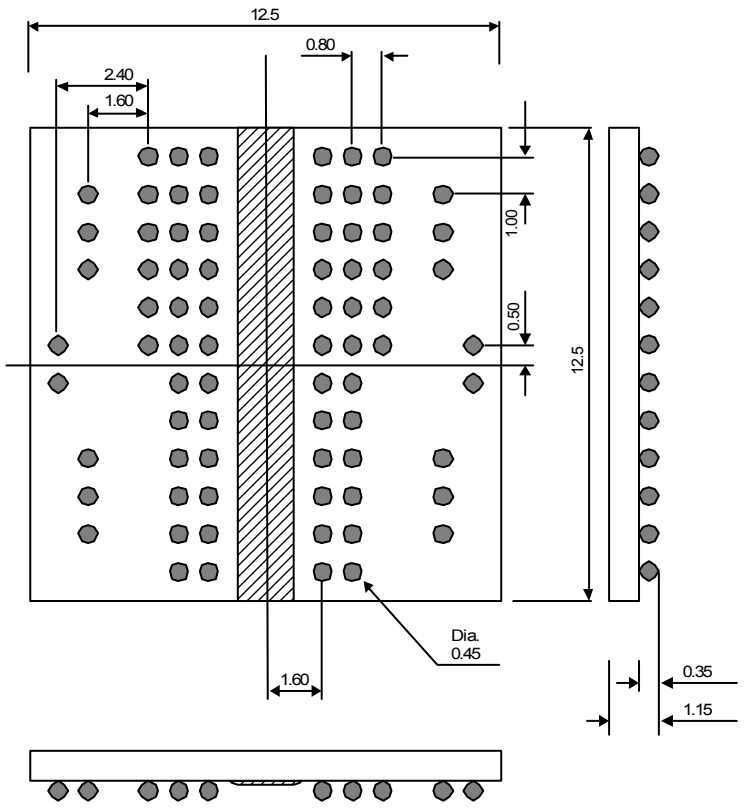
1. I/O slew rate is based on the lesser of the slew rates determined by either $V_{IH\ (AC)}$ to $V_{IL\ (AC)}$ or $V_{IH\ (DC)}$ to $V_{IL\ (DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

16. An I/O Delta Rise, Fall Derating table is used to increase t_{DS} and t_{DH} in the case where DQ, DM, and DQS slew rates differ.

Input Slew Rate	delta (t_{DS})	delta (t_{DH})	Unit	Notes
0.0 V/ns	0	0	ps	1,2,3,4
0.25 V/ns	+50	+50	ps	1,2,3,4
0.5 V/ns	+100	+100	ps	1,2,3,4

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH\ (AC)}$ to $V_{IL\ (AC)}$ or $V_{IH\ (DC)}$ to $V_{IL\ (DC)}$, similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: [1/(slew rate 1)] - [1/(slew rate 2)]
   For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns
   Delta rise, fall = (1/0.5) - (1/0.4) [ns/V]
   = -0.5 ns/V
   Using the table above, this would result in an increase in t_{DS} and t_{DH} of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

Package Dimensions (60 balls + 16 support balls; 0.8mmx1.0mm Pitch; CSP Package)



Note : All dimensions are typical unless otherwise stated.
Unit : Millimeters

Revision Log

Rev	Date	Modification
0.1	02/2004	Preliminary Release
0.2	03/2004	Add Idd specifications and condition